



H81H3-AM

Rev:1.0

ECS
CONFIDENTIAL

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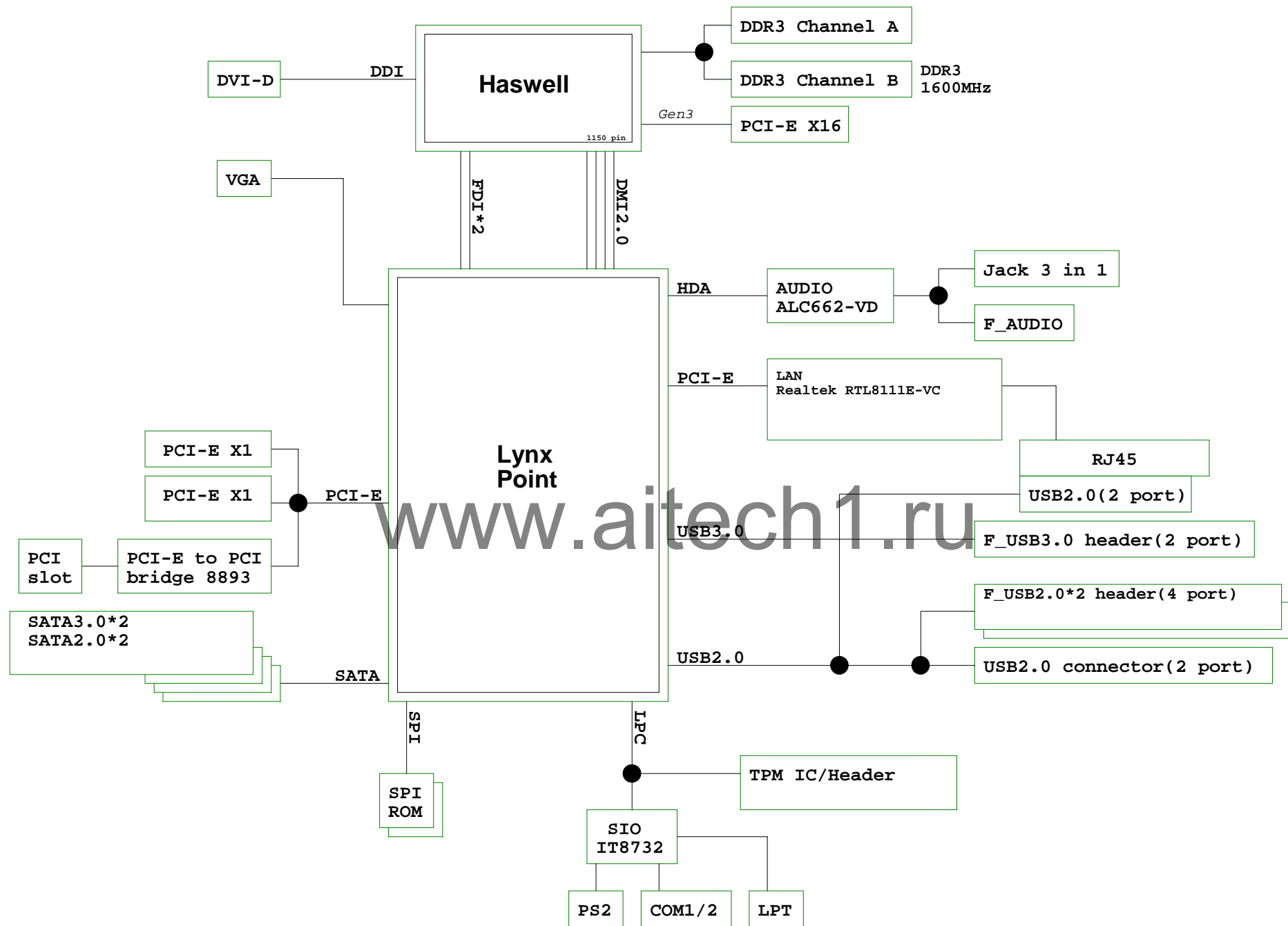
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REVISION HISTORY:

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PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO13	3VSB	LPC_PME	GPI
GPIO40	3VSB	USB_5VDUAL control (reserve)	Native
GPIO72	3VSB	USB_5VDUAL control	Native
GPIO45	3VSB	BIOS WP	Native
GPIO57	3VSB	BIOS WP	GPI
GPIO46	3VSB	WLAN_DIS_L	Native
GPIO61	3VSB	LPCPD_L	Native
GPIO27	ATX_3VSB	ILAN_WAKE_L	GPI
GPIO1	VCC3	OBR	GPI
GPIO6	VCC3	Thermal_SD	GPI
GPIO68	VCC3	TP_VGA	GPI
GPIO23	VCC3	HDPANEL_DETECT	Native
GPIO15	3VSB	PEX16_RST	GPO
DL, BIOS must be pro			
GPIO73	3VSB	case open(reserve)	PCIECLKRQ0#
GPIO24	3VSB	ME_Disable	GPO
GPIO19	VCC3	BOOT device detect	GPI
GPIO51	VCC3	BOOT device detect	GPO

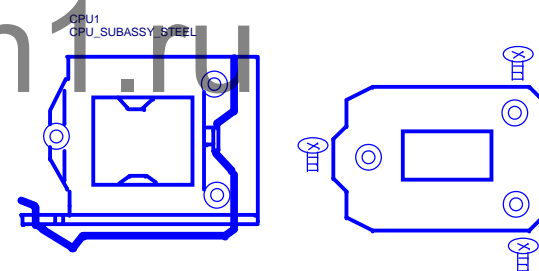
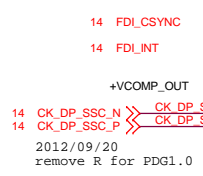
Interrupt mapping


Function	INT# port	PCIe*1 port	Device
PCI Bridge	INTB#	port 2	IC IT8893
LAN	INTC#	port 3	RTL8111E-VC
PCIEX1	INTD#	port 4	LPT integrate
PCIEX1	INTA#	port 5	LPT integrate
SATA	INTB#	NA	LPT integrate

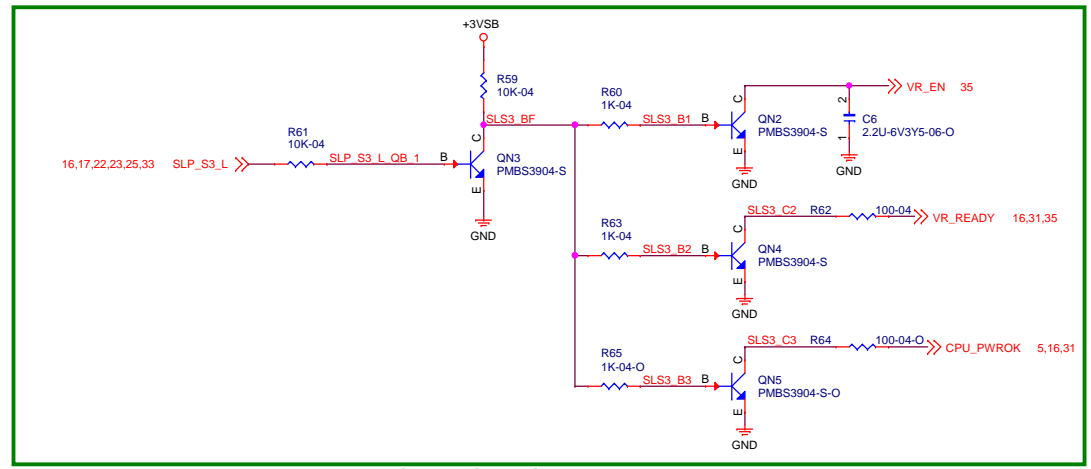
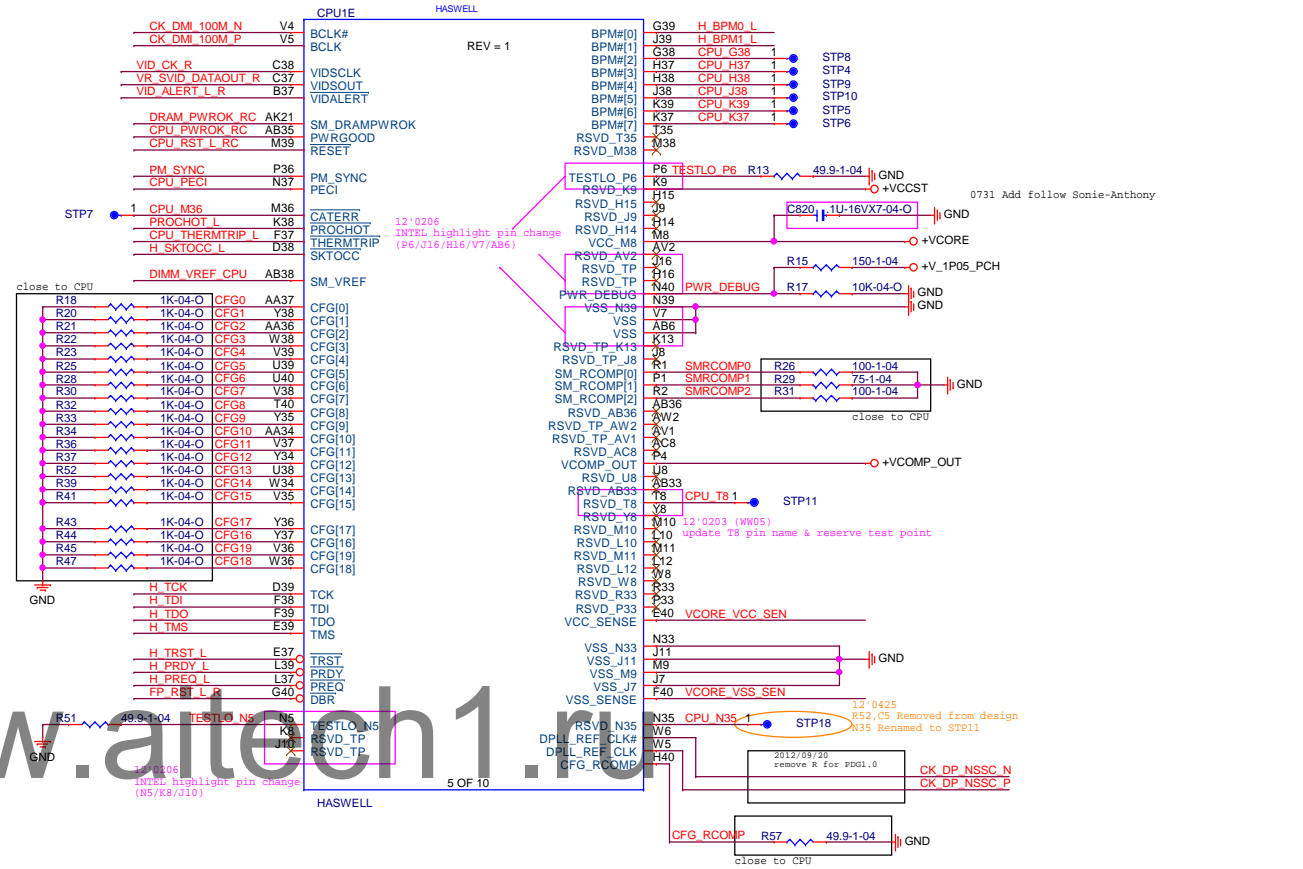
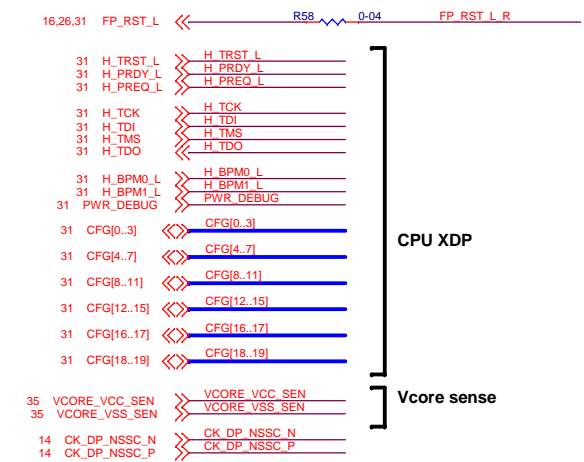
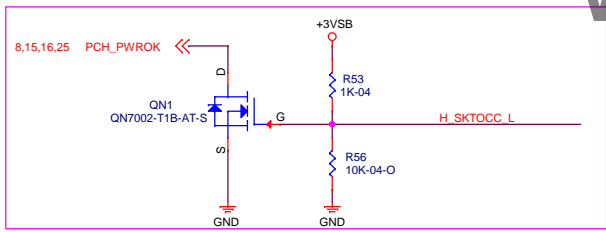
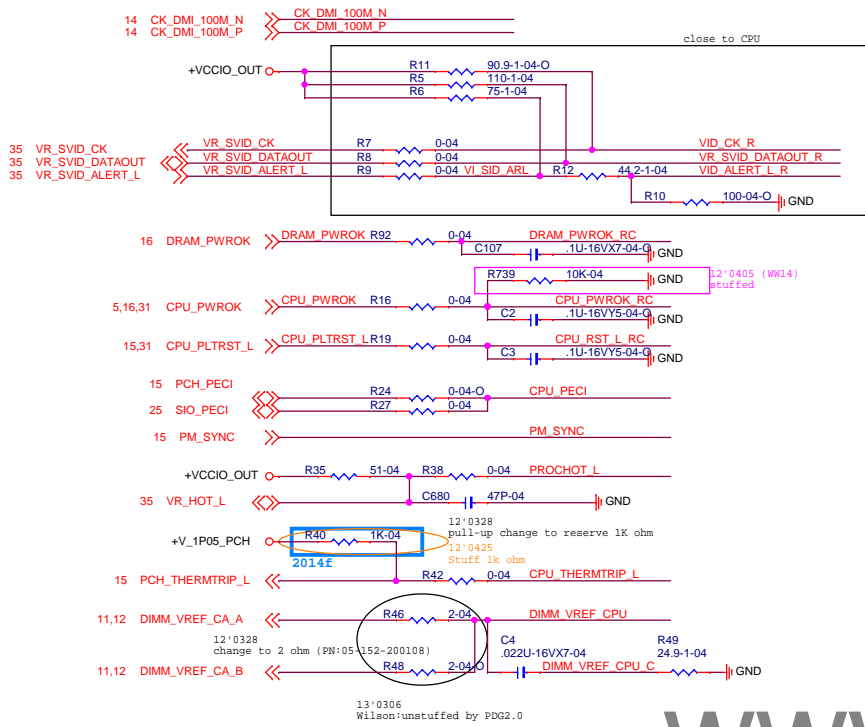
SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	Beep(reserve)	CIRRX2
GP31	3VSB	Thermal_SD	PWMOUT
GP35	3VSB	LED0	FAN_TAC4
GP37	3VSB	LED1	FAN_TAC3
GP70	VCC3	TPM Onboard detect	GPIO
GP71	VCC3	BOM detect	GPIO
GP73	VCC3	BOM detect	GPIO
GP74	VCC3	BOM detect	GPIO
GP75	VCC3	BOM detect	GPIO
GP76	VCC3	Thermal_HD_Auto_Switch	GPIO
GP46	3VSB	Acer Header	GPIO
GP47	3VSB	Acer Header	GPIO
GP40	3VSB	5VDUAL Switch	3VSB5W
RI1#	3VSB	LAN on MB wake up	RI1

BIOS must be pro to Native 3VSB5W



				
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Power Down Sequencing Circuit

11	M_DATA_A[0..63]	<<	M_DATA A[0..63]
11	M_DQS_A_P[0..7]	<<	M_DQS A P[0..7]
11	M_DQS_A_N[0..7]	<<	M_DQS A N[0..7]
11	M_MA_A[0..15]	<<	M_MA A[0..15]
11	M_BS_A[0..2]	<<	M_BS A[0..2]
11	M_CS_A_L[0..1]	<<	M_CS A L[0..1]
11	M_CKE_A[0..1]	<<	M_CKE A[0..1]
11	M_ODT_A[0..1]	<<	M_ODT A[0..1]
11	M_CLK_A_P[0..1]	<<	M_CLK A P[0..1]
11	M_CLK_A_N[0..1]	<<	M_CLK A N[0..1]
11	M_WE_A_L	<<	M_WE A_L
11	M_CAS_A_L	<<	M_CAS A_L
11	M_RAS_A_L	<<	M_RAS A_L

DDR3 CH.A

11	M_DATA_B[0..63]	<<	M_DATA B[0..63]
11	M_DQS_B_P[0..7]	<<	M_DQS B P[0..7]
11	M_DQS_B_N[0..7]	<<	M_DQS B N[0..7]
11	M_MA_B[0..15]	<<	M_MA B[0..15]
11	M_BS_B[0..2]	<<	M_BS B[0..2]
11	M_CS_B_L[0..1]	<<	M_CS B L[0..1]
11	M_CKE_B[0..1]	<<	M_CKE B[0..1]
11	M_ODT_B[0..1]	<<	M_ODT B[0..1]
11	M_CLK_B_P[0..1]	<<	M_CLK B P[0..1]
11	M_CLK_B_N[0..1]	<<	M_CLK B N[0..1]
11	M_WE_B_L	<<	M_WE B_L
11	M_CAS_B_L	<<	M_CAS B_L
11	M_RAS_B_L	<<	M_RAS B_L

DDR3 CH.B

6.11 DDR3_DRAMRST_L << DDR3_DRAMRST_L

**Attention

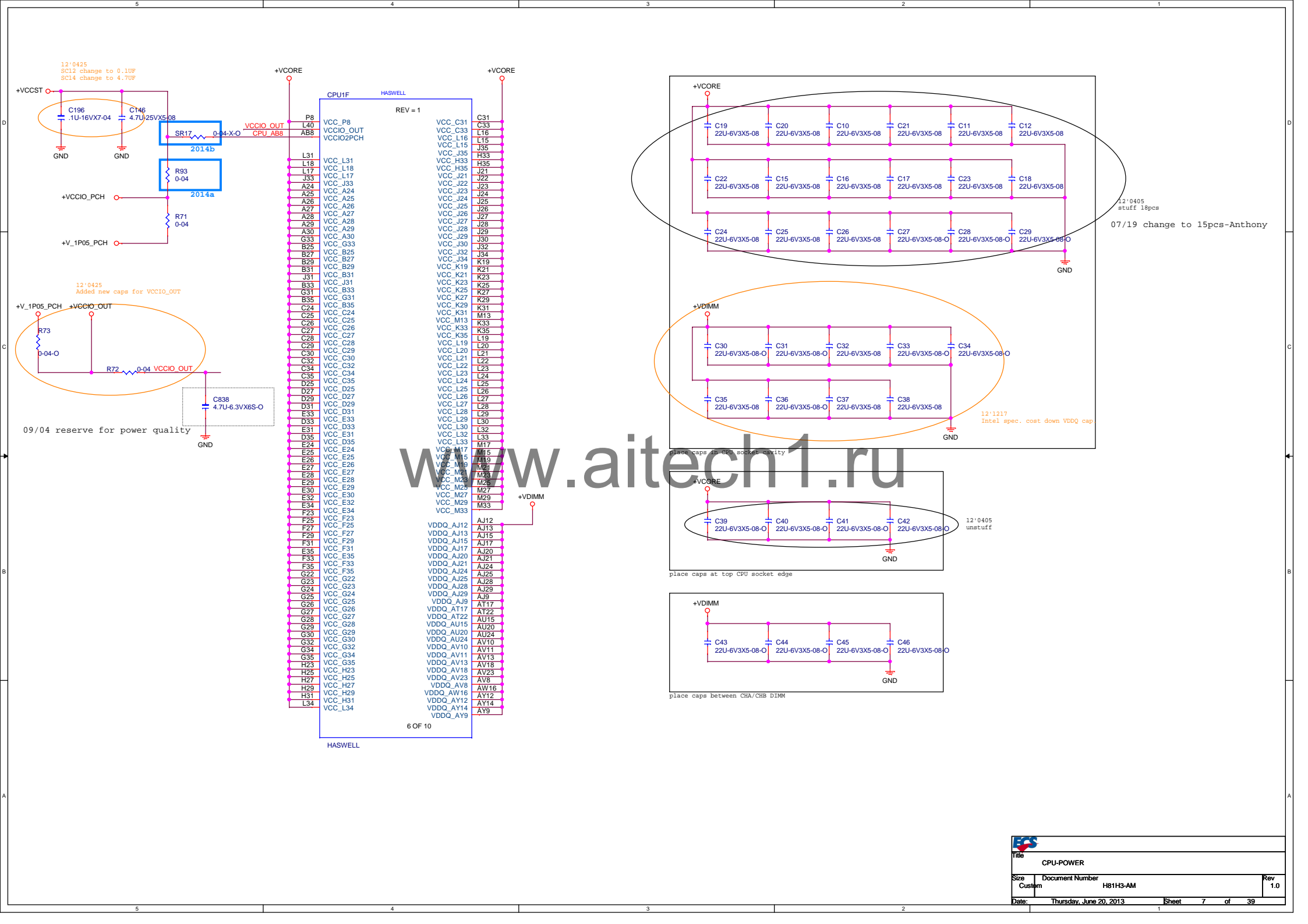
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M_DATA A1	AD39	SA_DQ[1]
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M_DATA A4	AD37	SA_DQ[4]
M_DATA A5	AD40	SA_DQ[5]
M_DATA A6	AF37	SA_DQ[6]
M_DATA A7	AF40	SA_DQ[7]
M_DATA A8	AH40	SA_DQ[8]
M_DATA A9	AH39	SA_DQ[9]
M_DATA A10	AK38	SA_DQ[10]
M_DATA A11	AK39	SA_DQ[11]
M_DATA A12	AH37	SA_DQ[12]
M_DATA A13	AH38	SA_DQ[13]
M_DATA A14	AK37	SA_DQ[14]
M_DATA A15	AK40	SA_DQ[15]
M_DATA A16	AM39	SA_DQ[16]
M_DATA A17	AM38	SA_DQ[17]
M_DATA A18	AP38	SA_DQ[18]
M_DATA A19	AP39	SA_DQ[19]
M_DATA A20	AM37	SA_DQ[20]
M_DATA A21	AM38	SA_DQ[21]
M_DATA A22	AP37	SA_DQ[22]
M_DATA A23	AP40	SA_DQ[23]
M_DATA A24	AV37	SA_DQ[24]
M_DATA A25	AW37	SA_DQ[25]
M_DATA A26	AU35	SA_DQ[26]
M_DATA A27	AV35	SA_DQ[27]
M_DATA A28	AT37	SA_DQ[28]
M_DATA A29	AU37	SA_DQ[29]
M_DATA A30	AT35	SA_DQ[30]
M_DATA A31	AW35	SA_DQ[31]
M_DATA A32	AV36	SA_DQ[32]
M_DATA A33	AU36	SA_DQ[33]
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M_DATA A45	AR3	SA_DQ[45]
M_DATA A46	AN2	SA_DQ[46]
M_DATA A47	AN1	SA_DQ[47]
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M_DATA A49	AL4	SA_DQ[49]
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M_DATA A55	AJ1	SA_DQ[55]
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M_DATA A57	AG4	SA_DQ[57]
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M_DATA A59	AE4	SA_DQ[59]
M_DATA A60	AC2	SA_DQ[60]
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M_DATA A62	AE2	SA_DQ[62]
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M_DQS A P6	AK3	SA_DQS[6]
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M_DQS A N31	AU32	SA_DQS[39]
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M_DQS A N41	AU32	SA_DQS[49]
M_DQS A N42	AU32	SA_DQS[50]
M_DQS A N43	AU32	SA_DQS[51]
M_DQS A N44	AU32	SA_DQS[52]
M_DQS A N45	AU32	SA_DQS[53]
M_DQS A N46	AU32	SA_DQS[54]
M_DQS A N47	AU32	SA_DQS[55]
M_DQS A N48	AU32	SA_DQS[56]
M_DQS A N49	AU32	SA_DQS[57]
M_DQS A N50	AU32	SA_DQS[58]
M_DQS A N51	AU32	SA_DQS[59]
M_DQS A N52	AU32	SA_DQS[60]
M_DQS A N53	AU32	SA_DQS[61]
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CPU1A

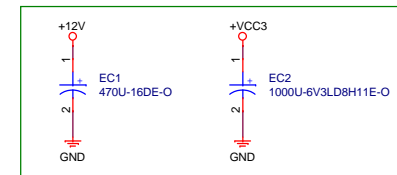
HASWELL

REV = 1

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SA_MA[1]	AV16 M_MA_A1
SA_MA[2]	AU16 M_MA_A2
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SA_MA[4]	AW17M_MA_A4
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SA_MA[6]	AV17 M_MA_A6
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SA_ODT[2]	AW9
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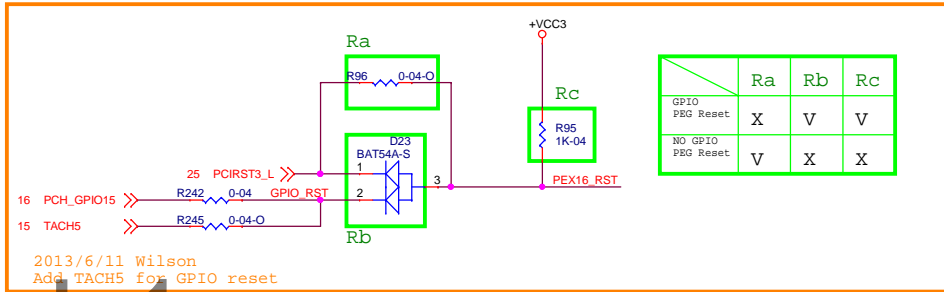
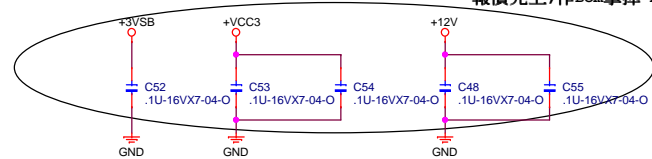


PCIE SPEC
VCC3:3A
12V:5.5A
3VSB:0.375A



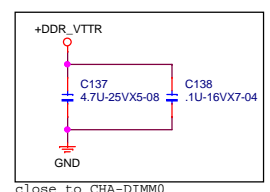
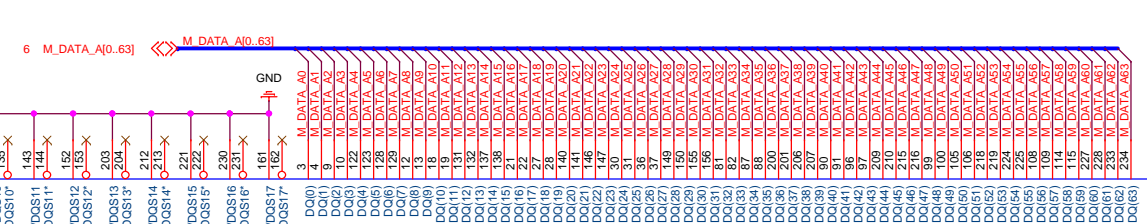
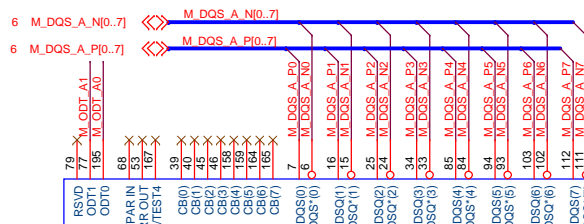
Between PCIE16 & PCIE1

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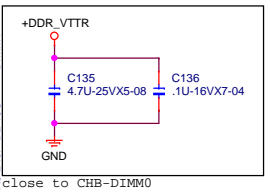
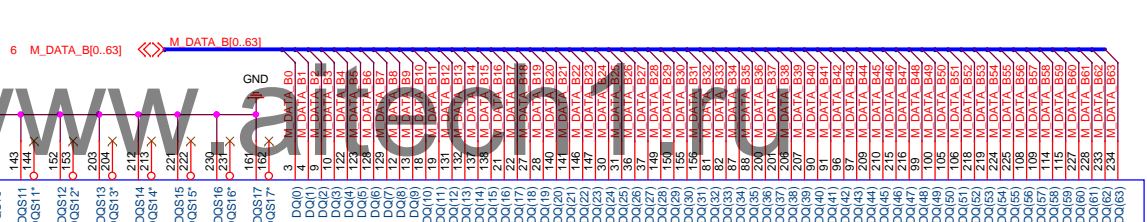
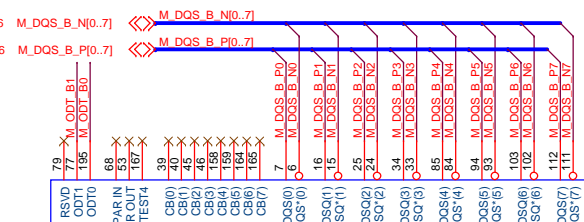
2013/6/11 Wilson
Add TACH5 for GPIO reset

2012/7/05
PCie Gen3 slot reset circuit update .

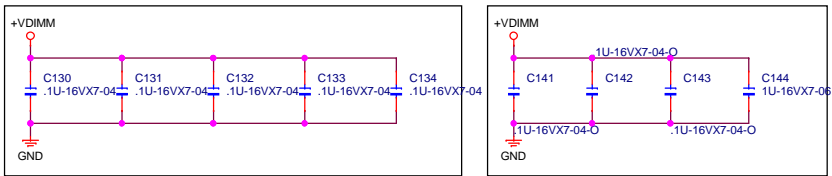
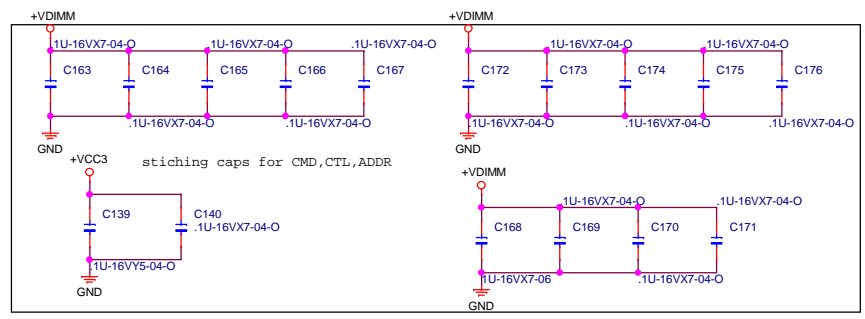


CHANNEL A DIMMs

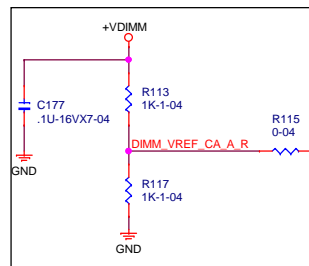
2013/1/8 by nick change remove DIMM



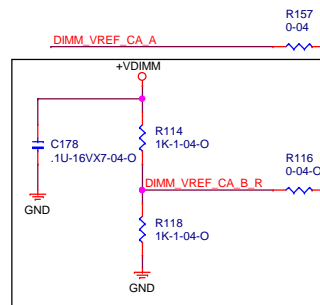
CHANNEL B DIMMs



Title			
DDR3-CHA			
Size	Document Number	Rev	
Custom	H81H3-AM	1.0	
Date:	Friday, June 21, 2013	Sheet	11 of 39



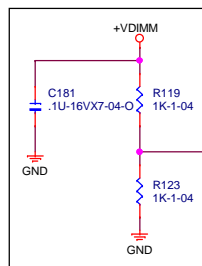
close to DIMM



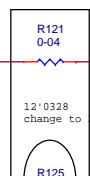
close to DIMM

0726 Fellow Intel PDG 1.0
VREF_CA Share-Anthony

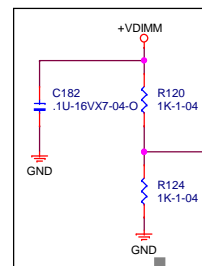
DIMM_VREF_CA Circuit



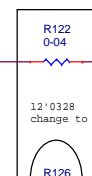
close to DIMM's vref



close to DIMM

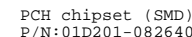
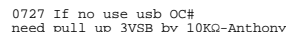
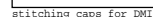


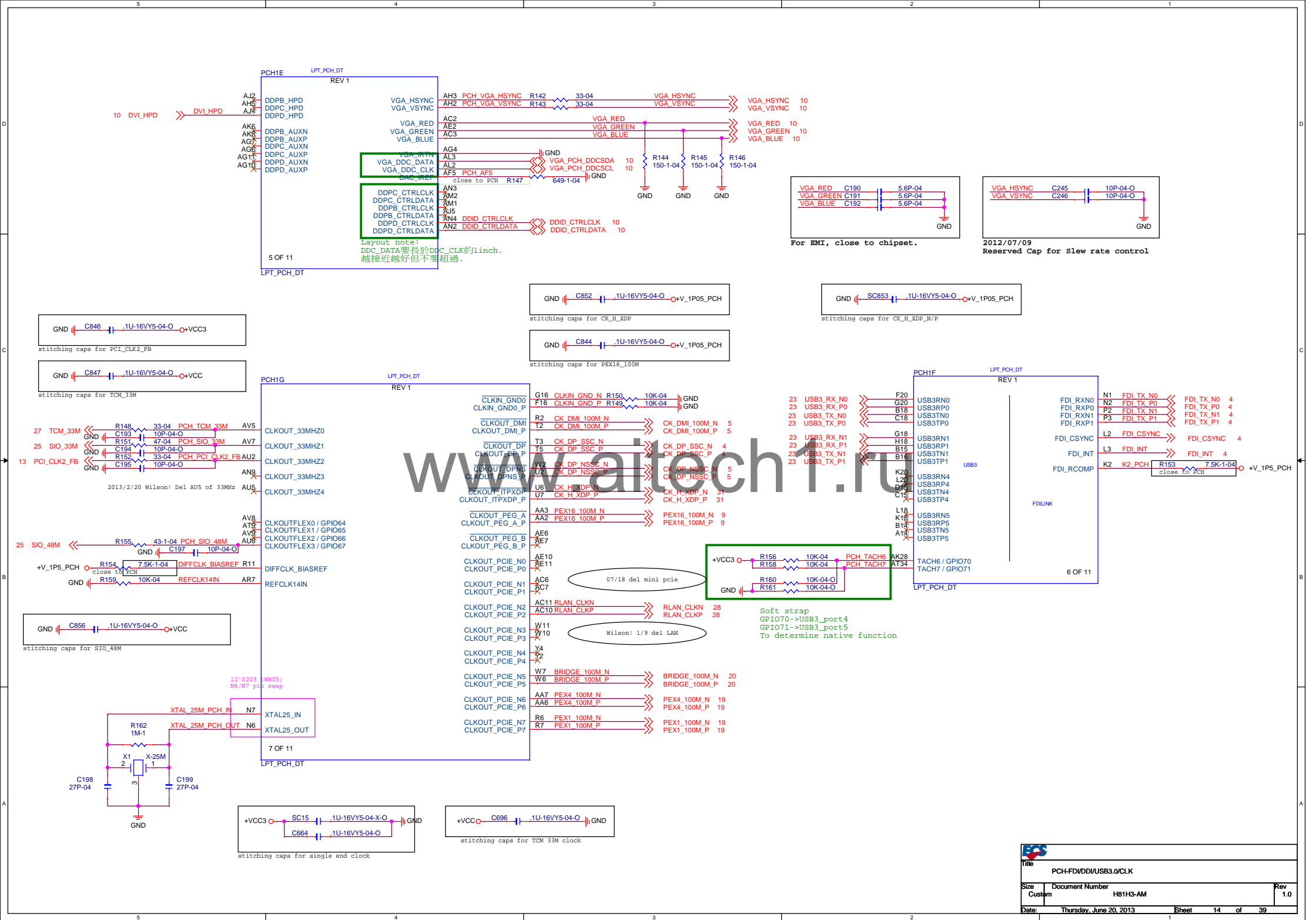
close to DIMM's vref

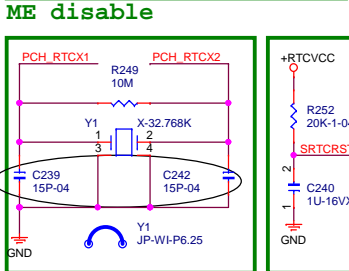
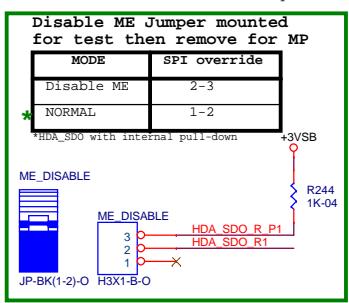
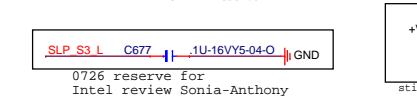
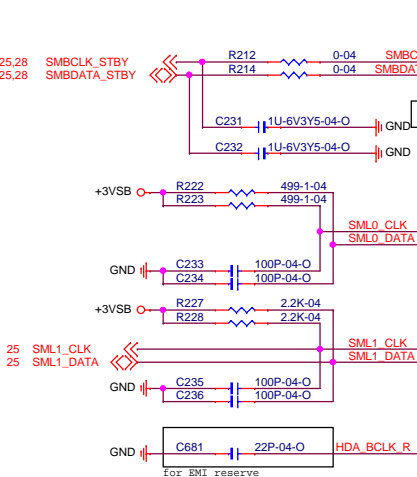
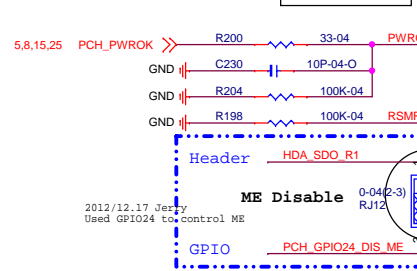
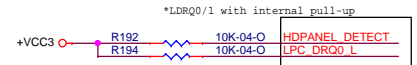


close to DIMM

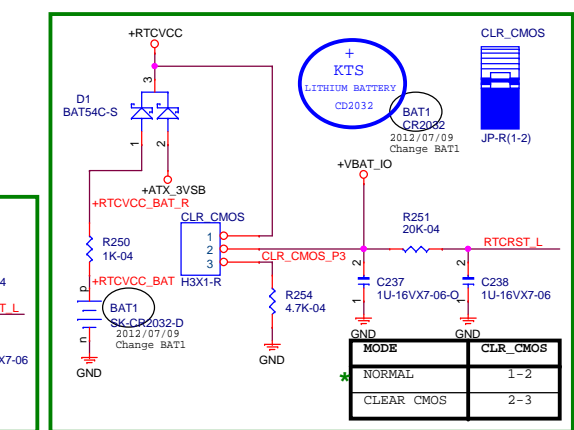
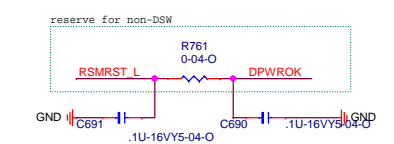
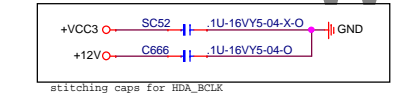
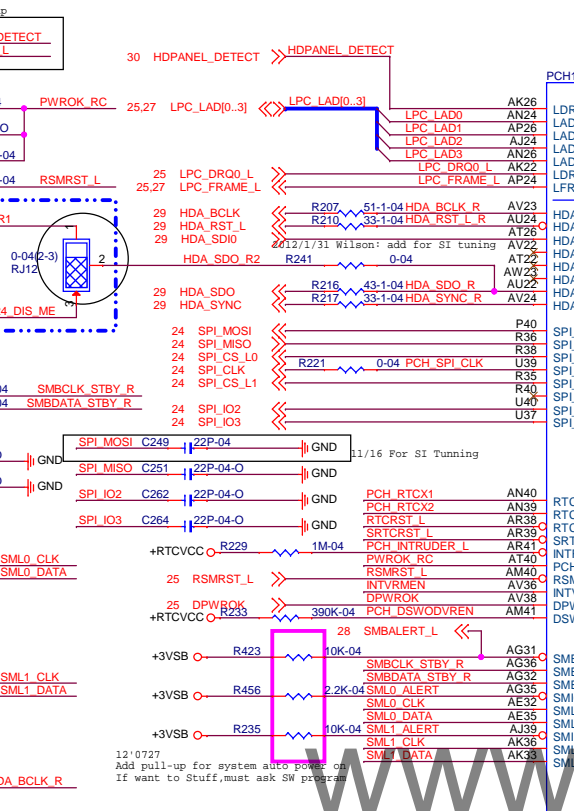
DIMM_VREF_DQ Circuit



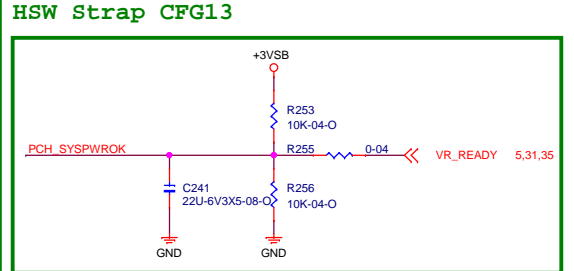
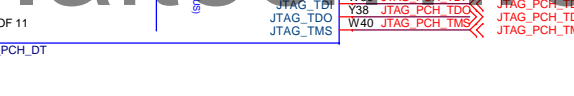
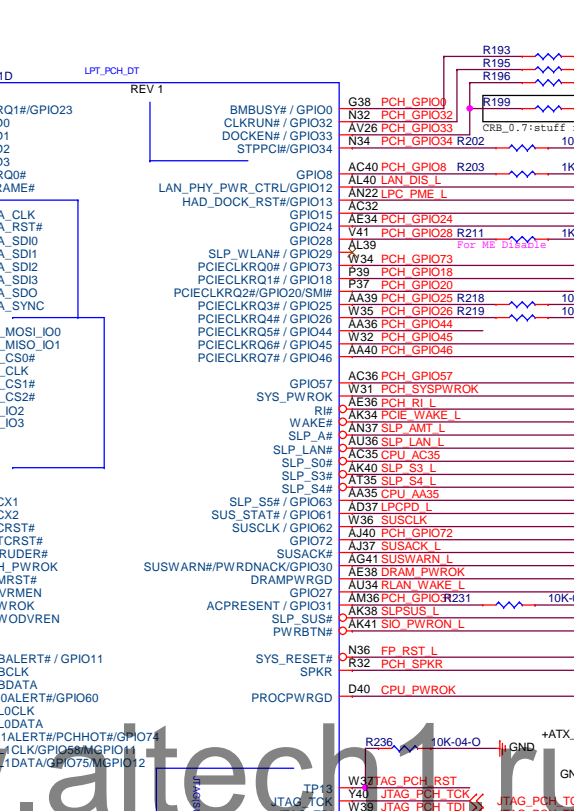




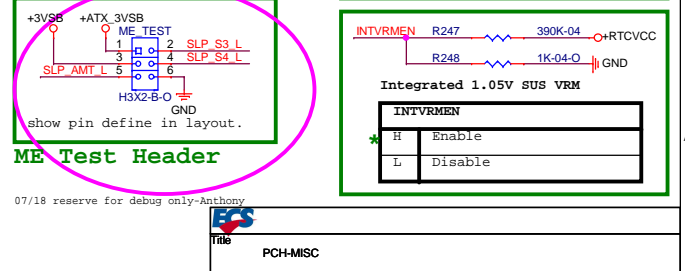
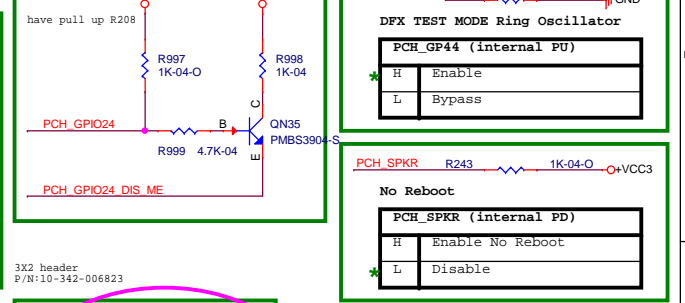
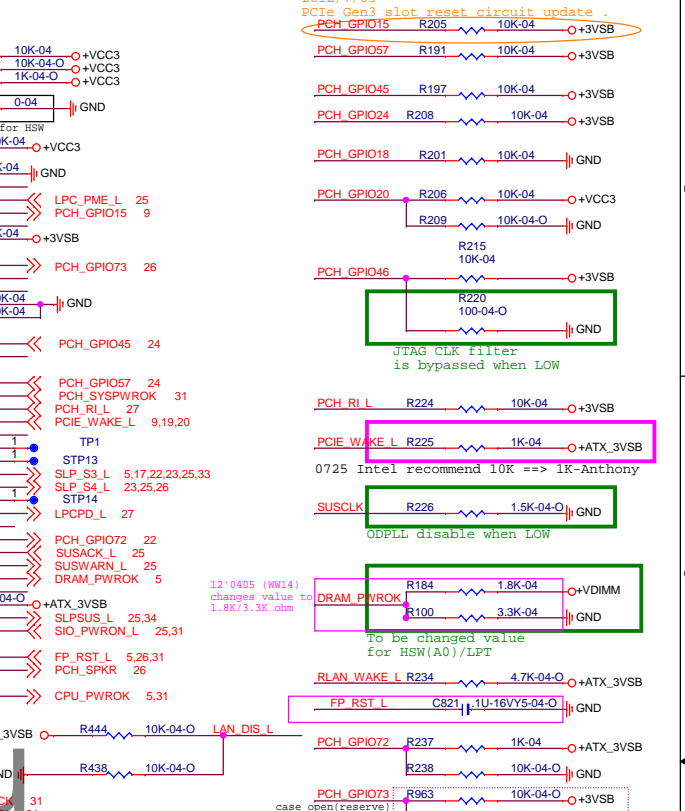
PCH Xtal
12/0528
C239 * C242 change to 15P for RTC test.



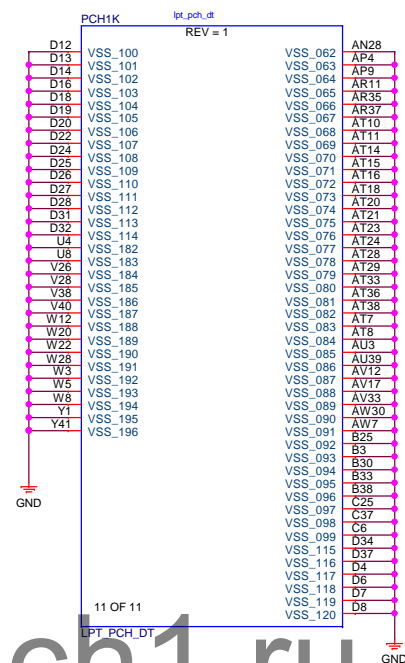
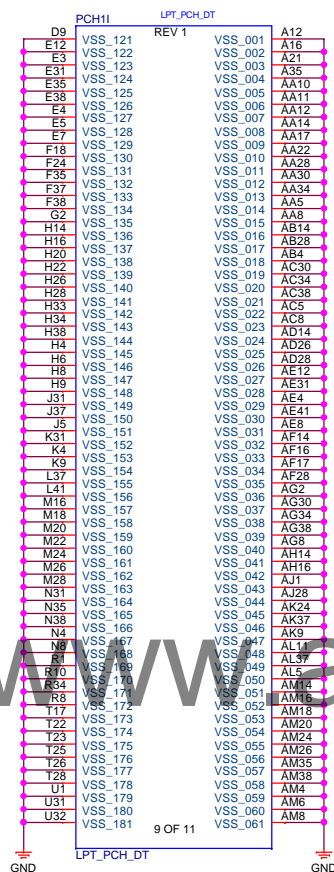
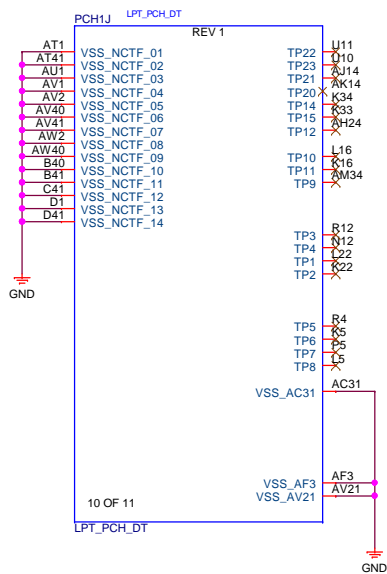
HSW Strap CFG13
2012/07/09
Change BAT1



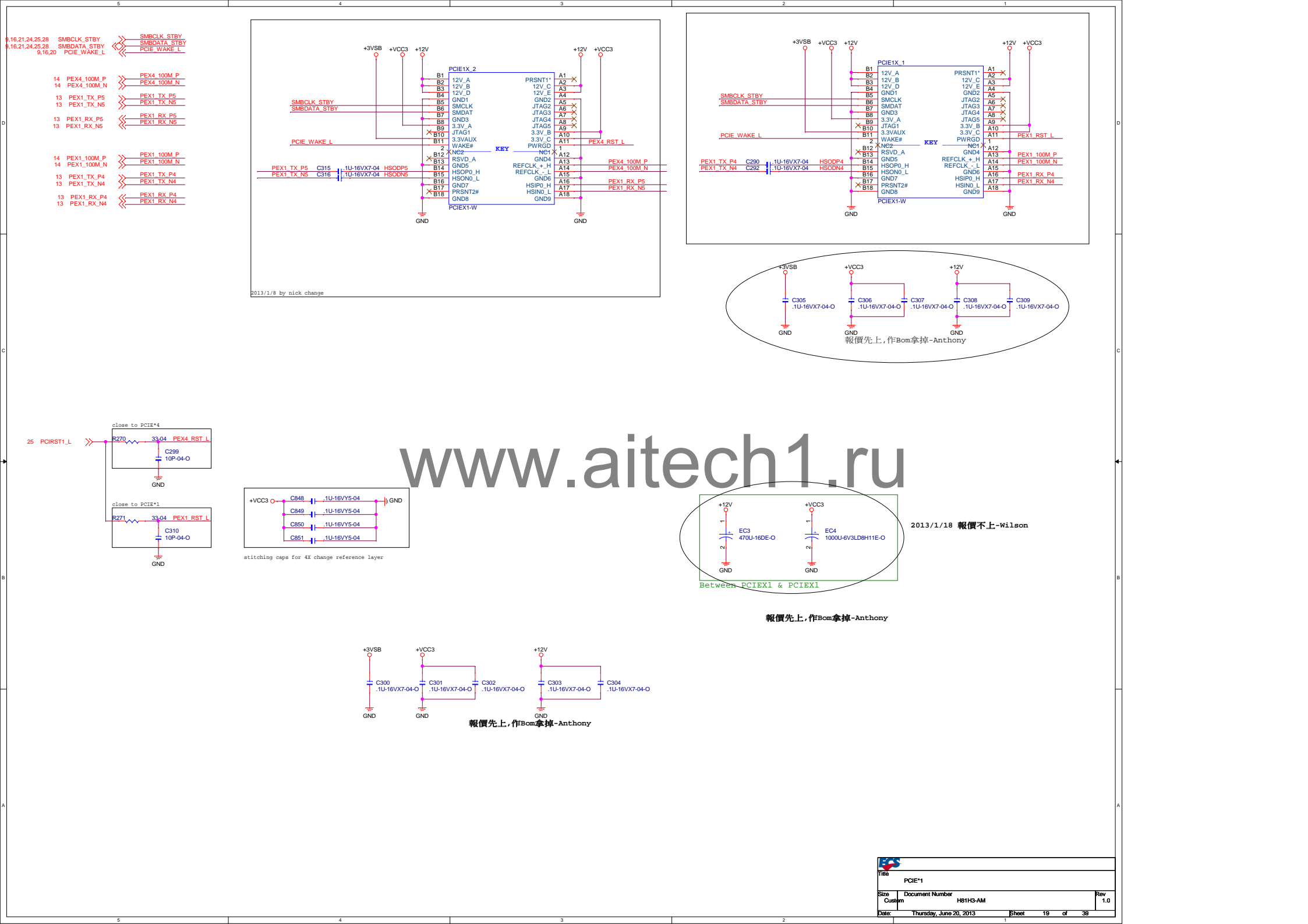
PCH Xtal
12/0528
C239 * C242 change to 15P for RTC test.

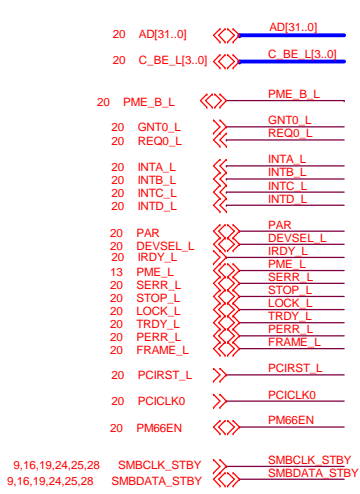


PCH Xtal
12/0528
C239 * C242 change to 15P for RTC test.

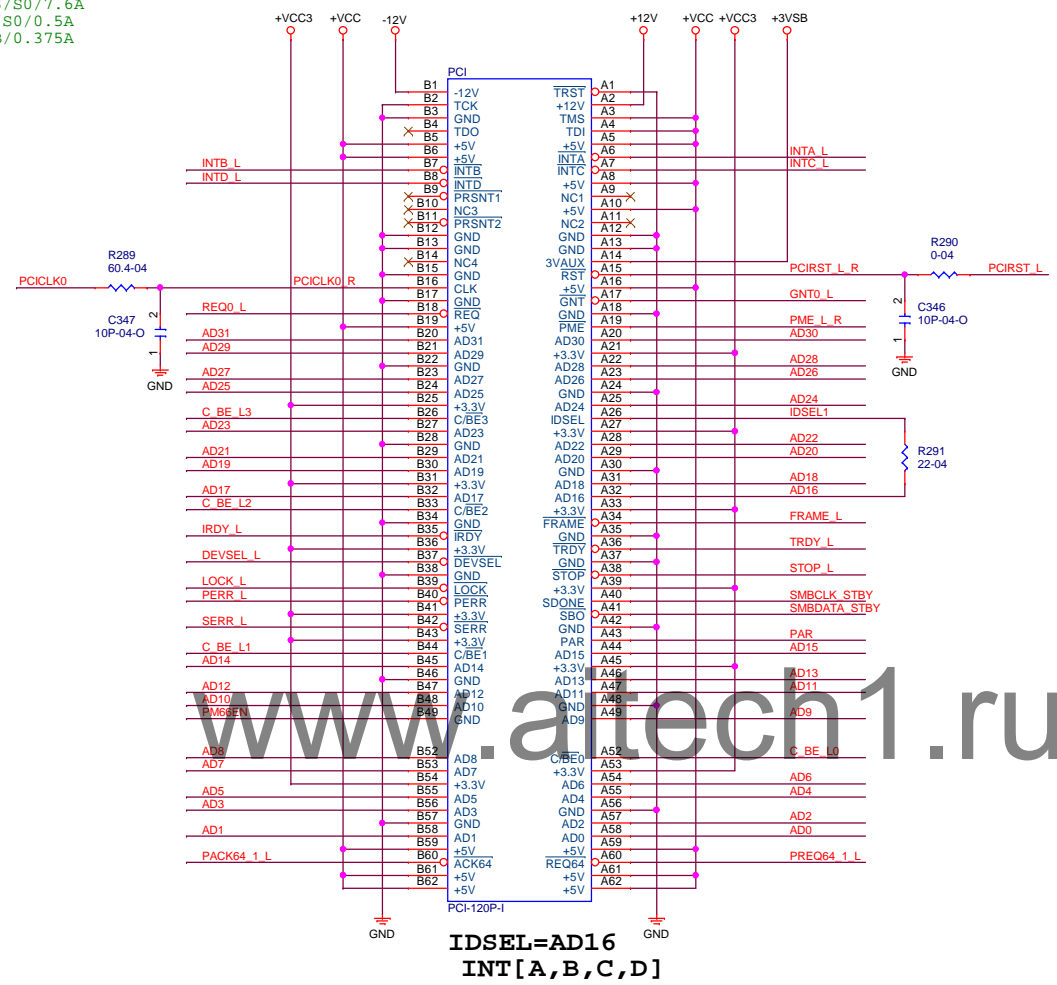


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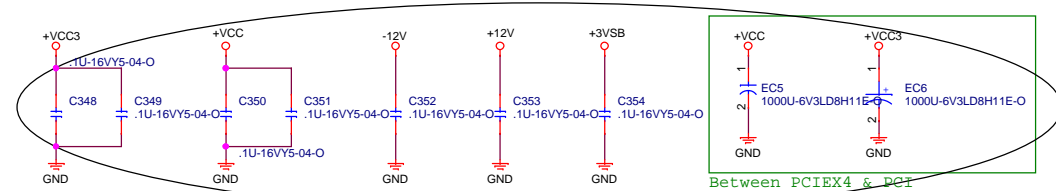




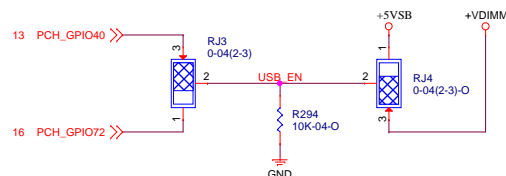
****PCI Slot****
 +VCC/S0/5A
 +VCC3/S0/7.6A
 +V12/S0/0.5A
 +3VSB/0.375A



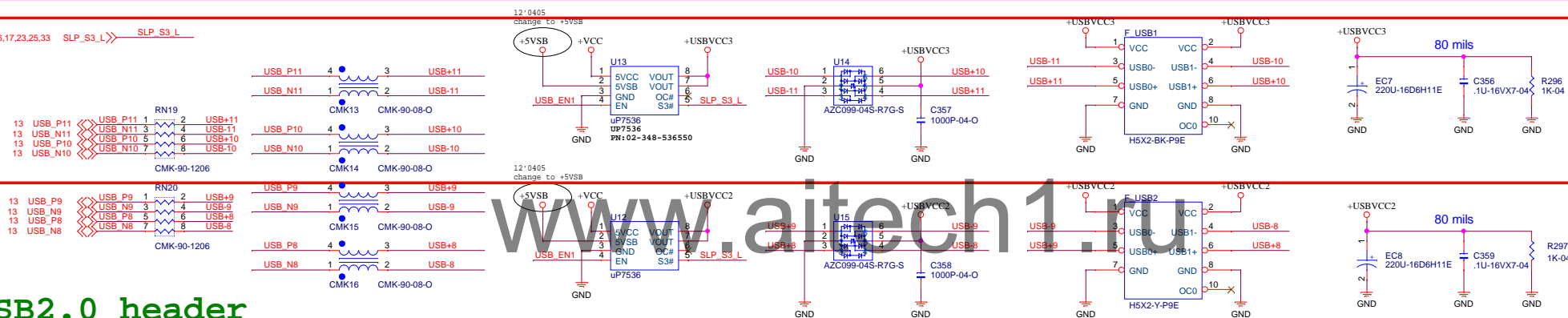
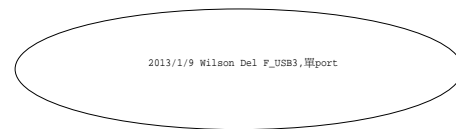
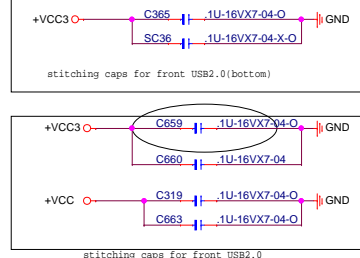
IDSEL=AD16
 INT[A,B,C,D]



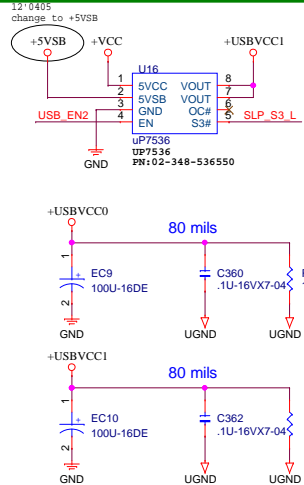
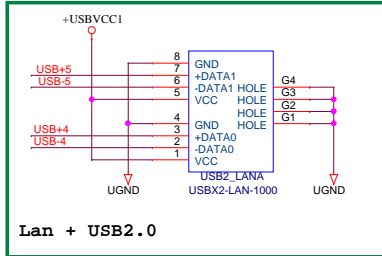
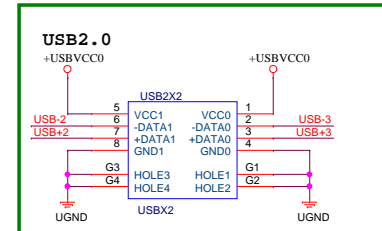
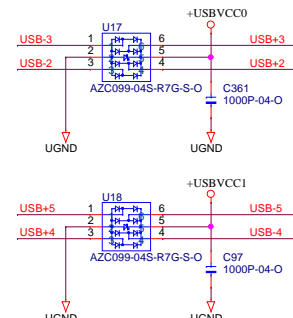
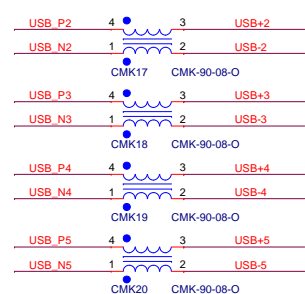
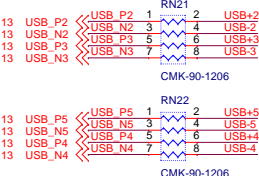
報價先上, 作Bom拿掉-Anthony



	uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
	5VSB	0ohm (2-3)	NA	5 Volt	
*	GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	



USB2.0 connector

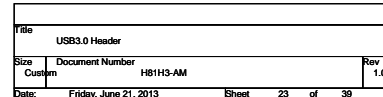


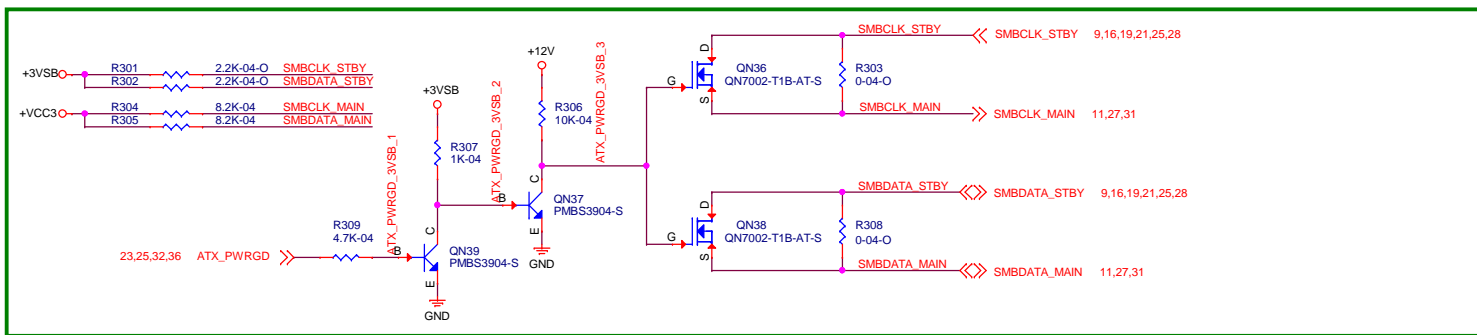
3. OC[3:0]# should be connected with USB 2.0 ports 0 - 7 and any 4 of USB 3.0 ports 1 - 6.
4. OC[7:4]# should be connected with USB 2.0 ports 8 - 13 and any 4 of USB 3.0 ports 1 - 6.

need to measure S

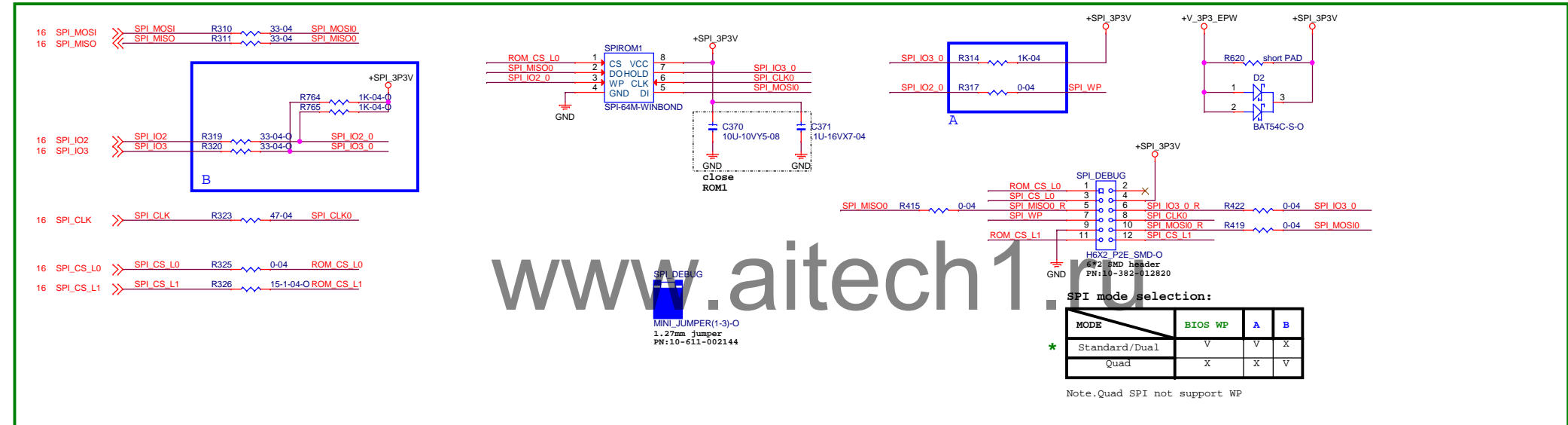


5V_DUAL





SMBus Logic Circuit



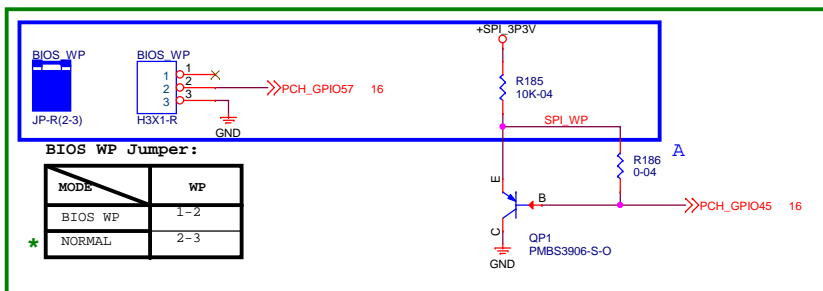
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SPI mode selection:

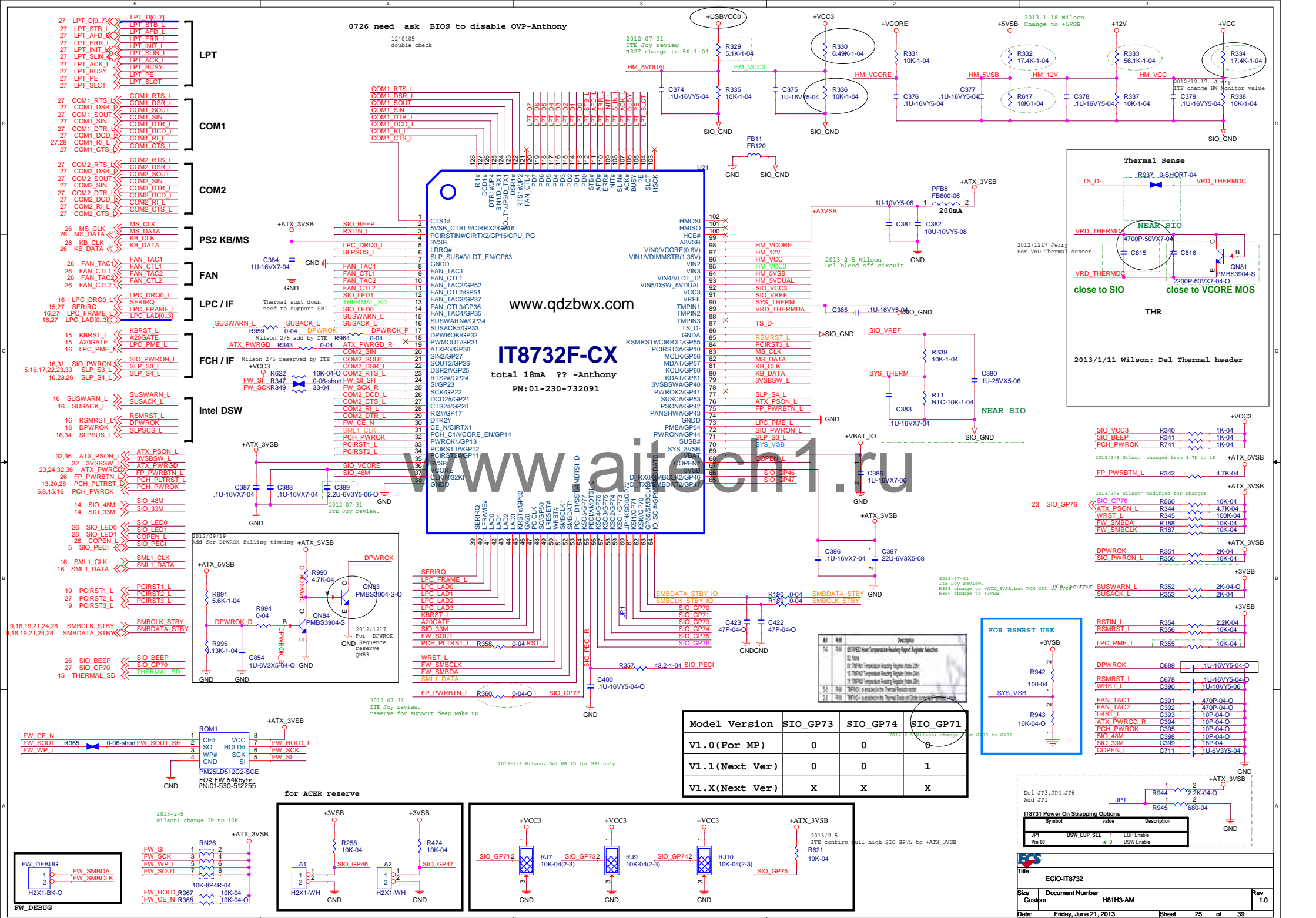
MODE	BIOS WP	A	B
Standard/Dual	V	V	X
Quad	X	X	V

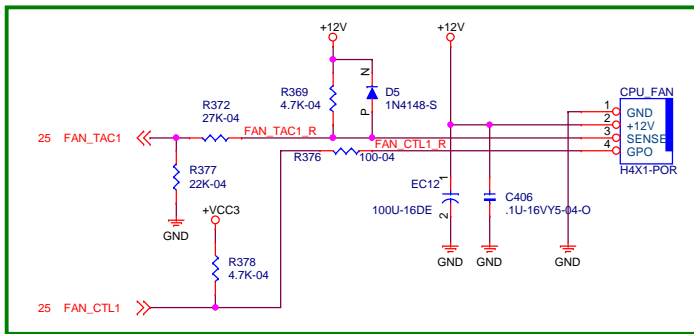
Note: Quad SPI not support WP

SPI ROM

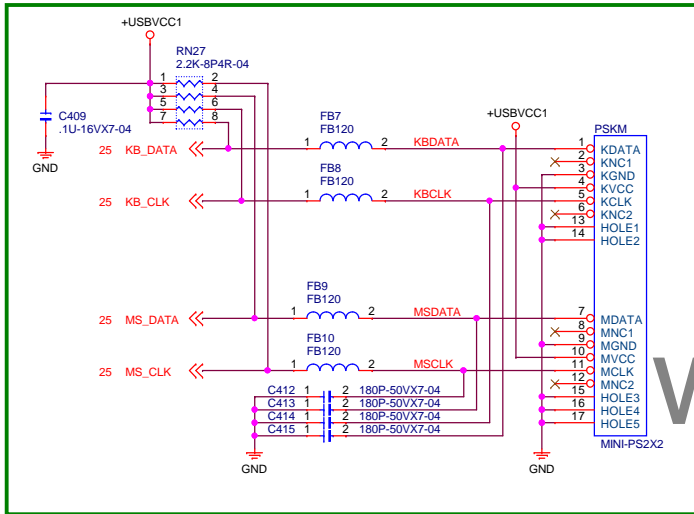


BIOS WP

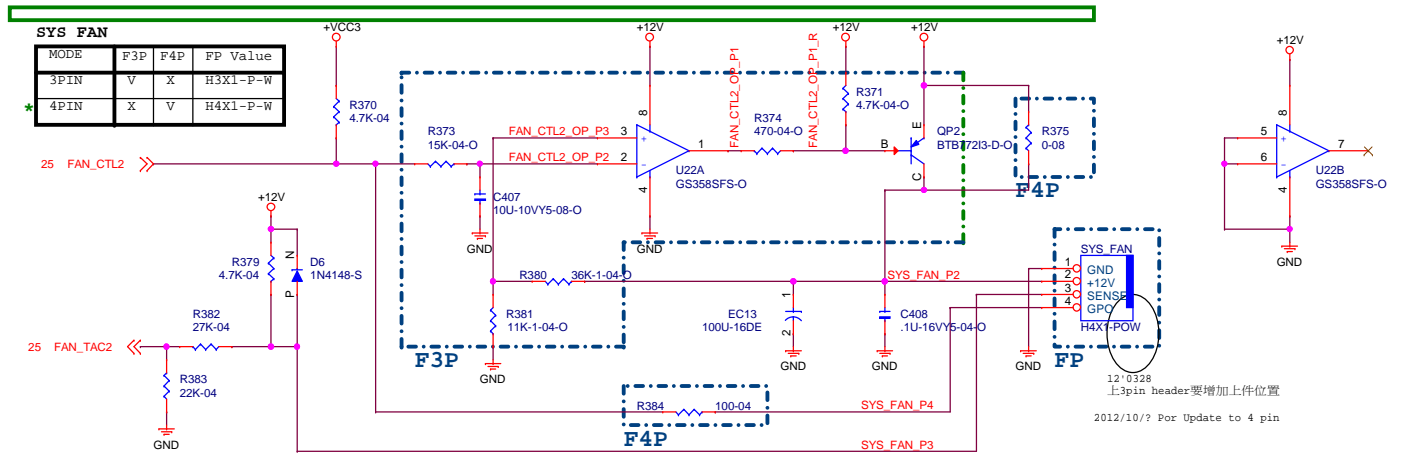




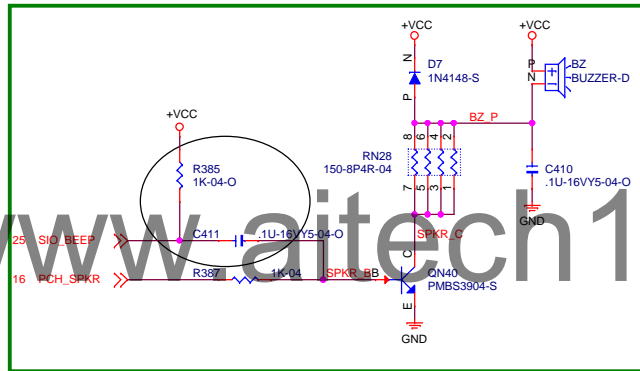
CPU_FAN 4 pin circuit



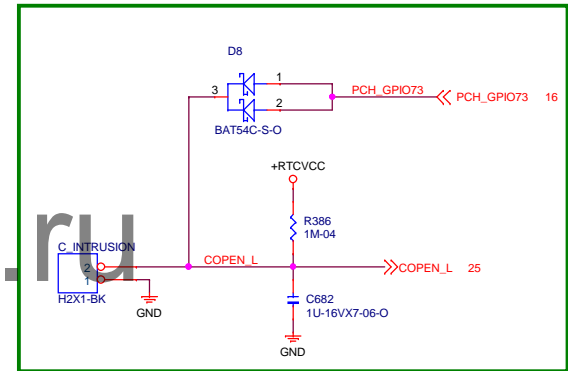
PS2 circuit



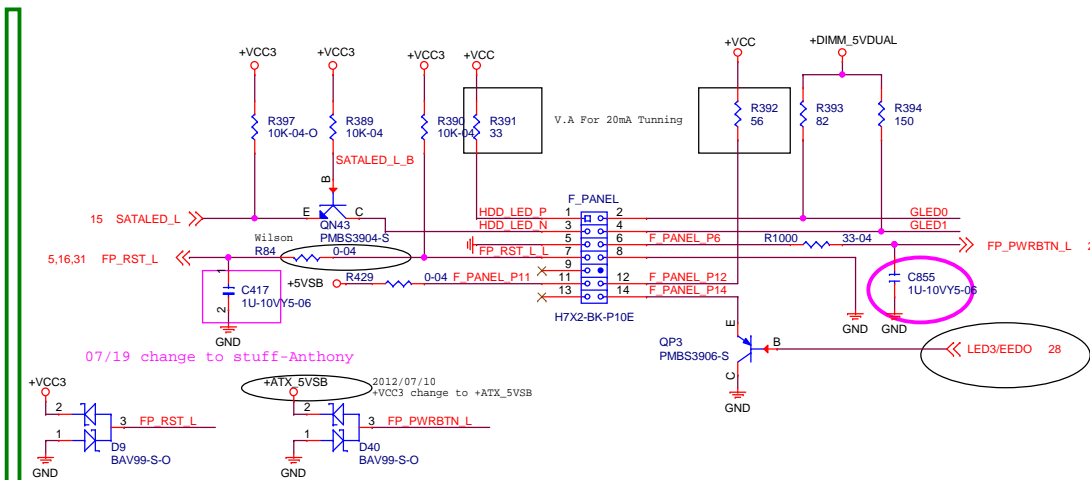
SYS_FAN 3/4 pin co-layout circuit



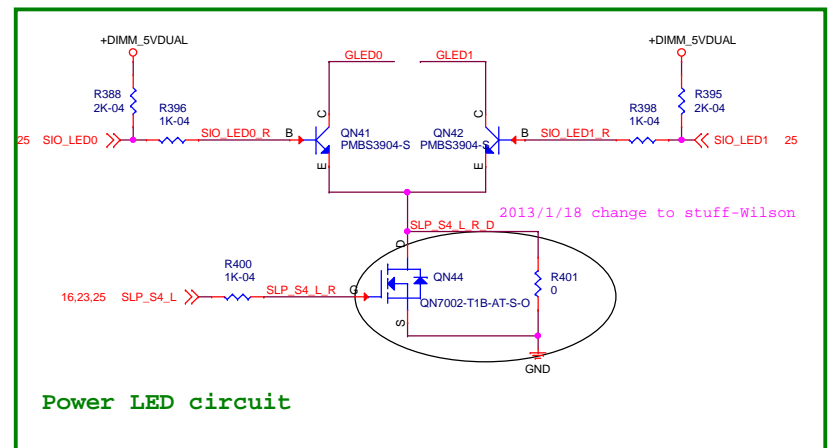
Buzzer circuit



Case open circuit



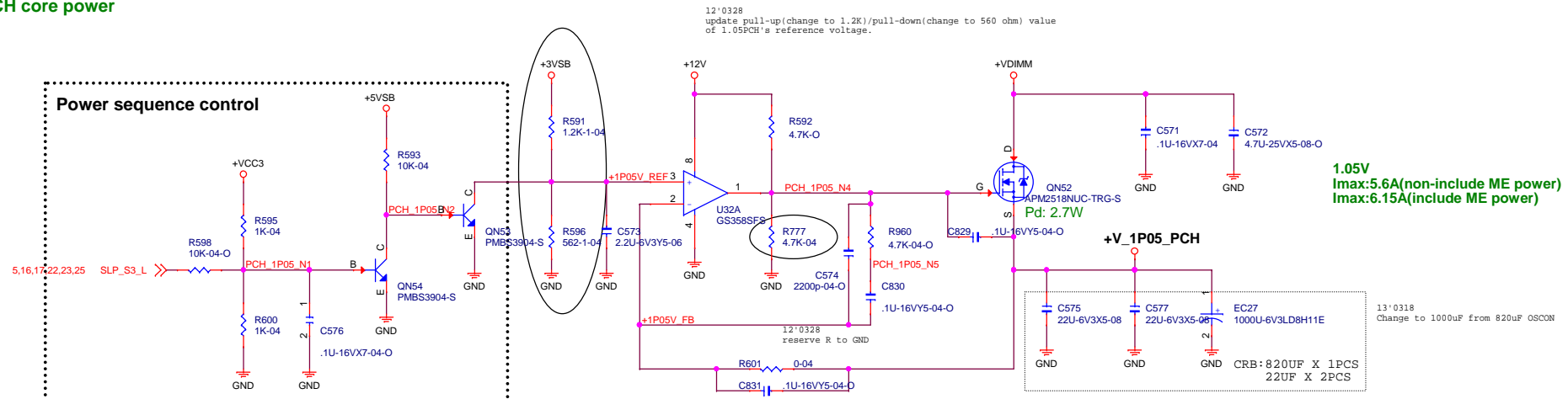
Front Panel circuit



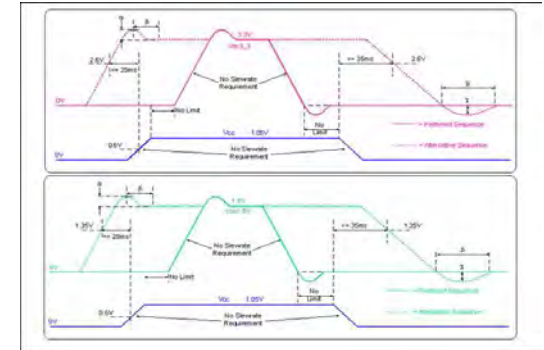
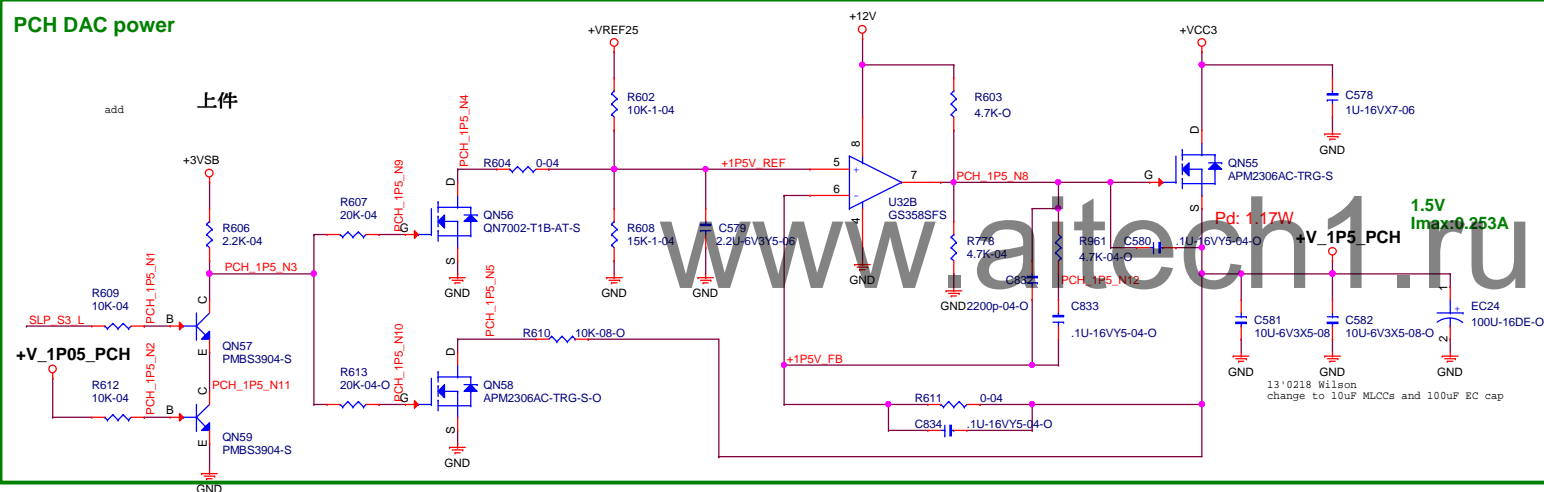
Power LED circuit

PCH core power

Power sequence control

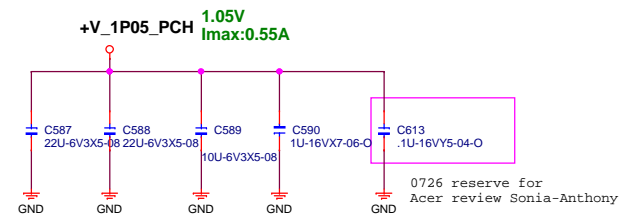


PCH DAC power



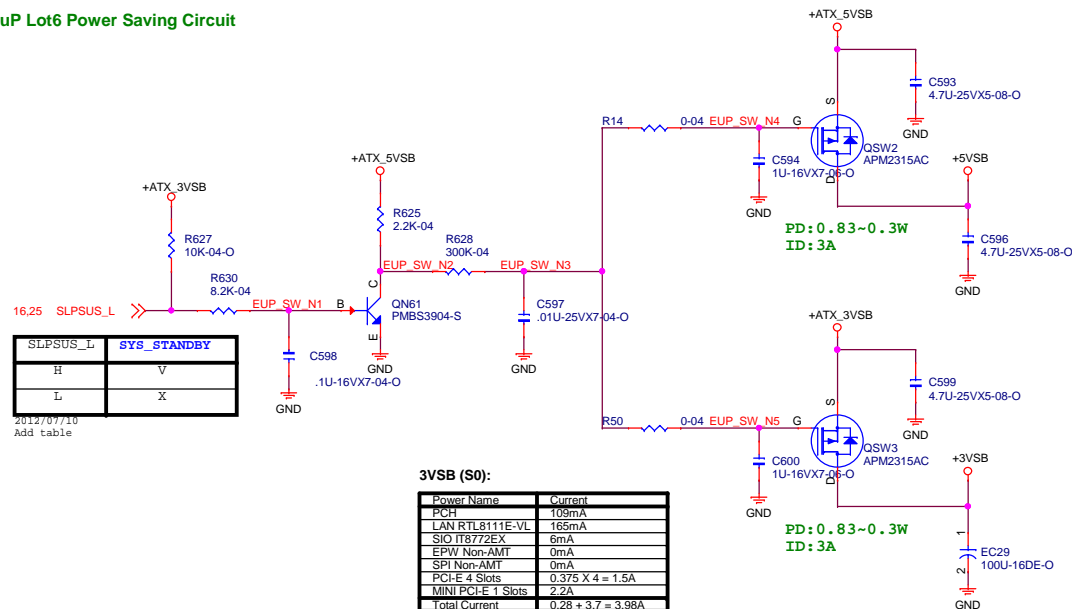
PCH ME power

2013/1/10 Wilson: Del ME POWER circuit

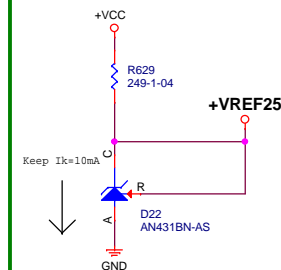
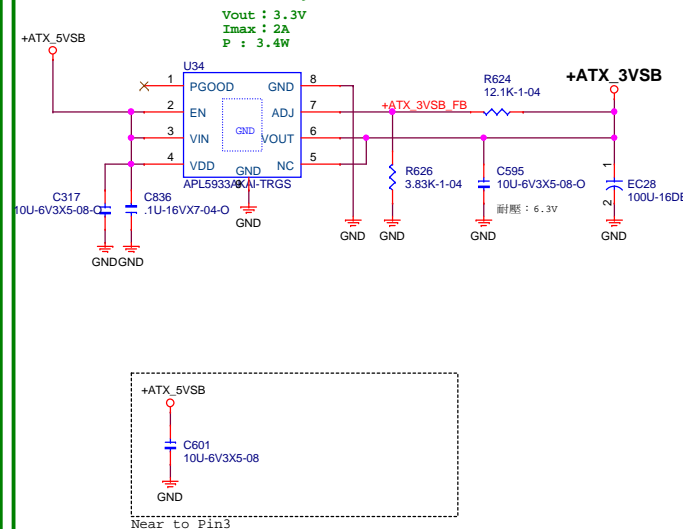


Title			DC/DC PCH_1.5V/PCH_ME_1.05V
Size	Document Number	Rev	
Custom	H81H3-AM	1.0	
Date:	Thursday, June 20, 2013	Sheet	33 of 39

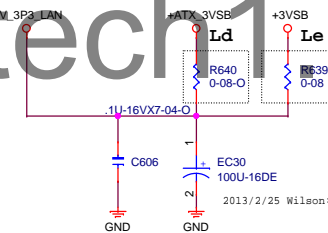
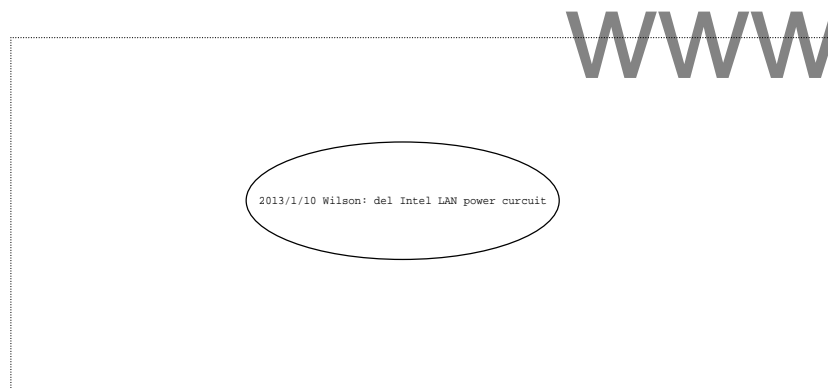
EuP Lot6 Power Saving Circuit



+3V Standby



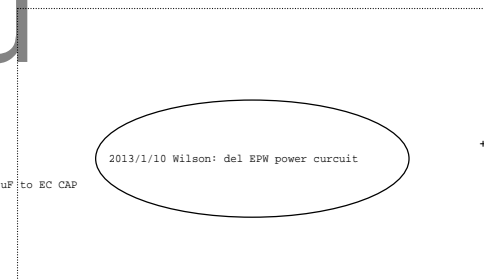
LAN Power Circuit



LAN Power Source

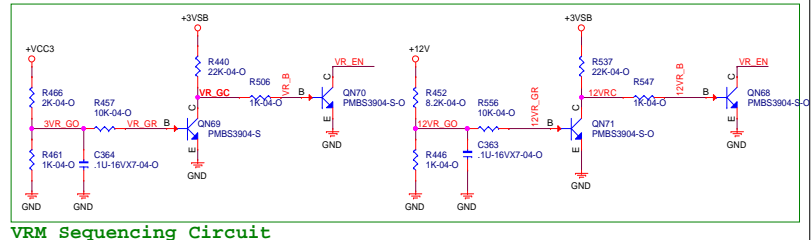
	EUP Enable G3--->X5, X5	La	Lb	Lc	Ld	Le
Intel LAN	can wake up	V	V	X	X	
	can't wake up	V	X	V		
Realtek LAN	can wake up				V	X
	can't wake up				X	V

SPI ROM & PCH Power Circuit

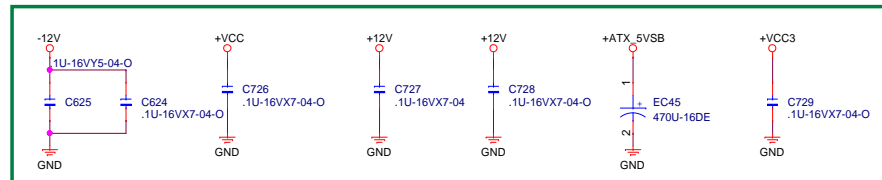



+VCC3_EPW	Ld	Le	Lf
Intel LAN	X	V	X
Realtek LAN	V	X	X
Intel LAN(Cost down)	X	X	V

ISL95820 FOR VR12.5 RFQ SCHEMATIC



Title			
VR12.5 SOLUTION ISL95818 SUGGEST SCHEMATIC			
Size	Document Number		Rev
C	H8THS-AM		1.0
Date:	Friday, June 21, 2013	Sheet	35 of 39

[illegible]

				
Title				
ATX 24P				
Size	Document Number			Rev
Custom	H81H3-AM			1.0
Date:	Friday, June 21, 2013		Sheet	36 of 39

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ATX24P					ATX4P
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%	12V +/-5%

Switching
NCP81102
3 phases

5VDUAL
P/N MOS

Switching
RT8120F

LDO
APL5336

DDR3 DIMM 1600MHz (2)	
VDIMM	6A(TDC)
VDIMM_VTT	1A

OP
Linear

OP
Linear

Intel Haswell CPU		
VCORE	SVID	105A(95W)
VDIMM	1.5V	4.5A
VCCIO_PCH	1V	TBD

Intel Lynx Point (TDP 4.1W)		
VCC	1.05V	1.29A
V_PROC_IO	1.05V	4mA
VccIO	1.05V	3.629A
VccCLK	1.05V	306mA
VccASW(ME)	1.05V	670mA
VccADAC1_5	1.5V	70mA
VccVRM	1.5V	179mA
VccCLK3_3	3.3V	55mA
VccADAC3_3	3.3V	13.3mA
VccSPI	3.3V	22mA
VccDSW3_3	3.3V	15mA
VccSUS3_3	3.3V	261mA
VccSUSHDA	3.3V	10mA
VccRTC	3.3V	6uA(G3)
DcpSUS1	1.05V	98mA
DcpSUS2	1.05V	28mA
DcpSUS3	1.05V	476mA

Battery
3V

LAN		
VDD3P3	3.3V	177mA
VDD10	1V	300mA

FAN		
CPU_FAN	+12V	1A
SYS_FAN	+12V	1A

SIO IT8732		
3VSB	3.3V	TBD
VCC3	3.3V	TBD
Battery 3.3V	3.3V	TBD

AUDIO ALC662-VD		
DVDD 3.3V	3.3V	11mA
AVDD	5V	42mA
Internal LDO		

PCI Slot per	
3.3V	7.6A(S0)
12V	0.5A(S0)
5V	5A
3.3Vaux	0.375A

X16 PCIE Slot per	
3.3V	3A(S0)
12V	5.5A(S0)
3.3Vaux	0.375A

X1 PCIE Slot per	
3.3V	3A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A

5VDUAL
UP7537

5VDUAL
UP7536

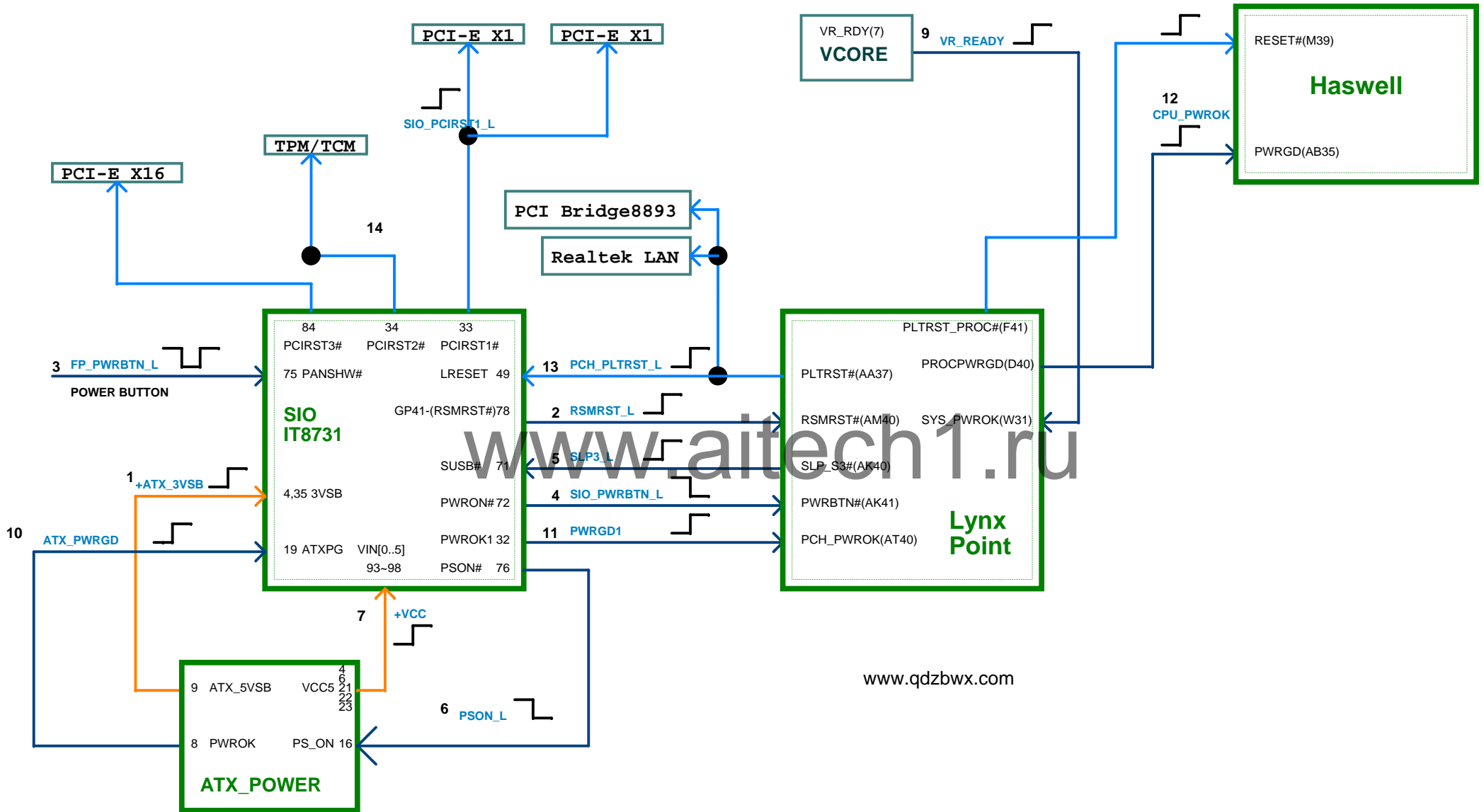
each USB3.0	
VDD	5VDual
	0.9A

each USB2.0	
VDD	5VDual
	0.5A

PS/2	
	5VDual
	275mA

ATX_3VSB
VCC3

VCC3
ATX_5VSB



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